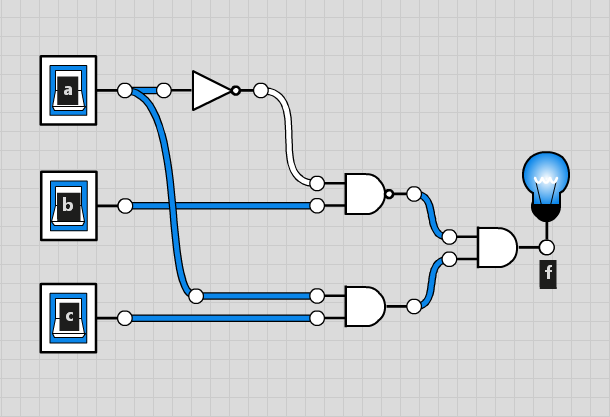
**Lab 0 Pre-lab Report:**

**Part I:**

Design a circuit that has in three inputs (a , b and c) and one output (f), where f performs the following logic function: f = ab + ac.

**Logic function: f = a·b + a·c**

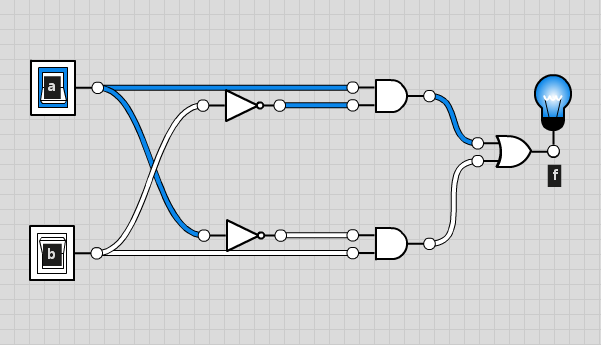
**Truth Table: Circuit graph:**

|  |  |  |  |
| --- | --- | --- | --- |
| **a** | **b** | **c** | **f** |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

**Part II:**

Design a circuit that has two inputs (x and y) and one output (f). This circuit makes f true (1) when x and y are different, and makes f false (0) when they are the same.

**Logic function: f = a’·b + a·b’**

**Truth Table: Circuit graph:**

|  |  |  |
| --- | --- | --- |
| **x** | **y** | **f** |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**Part III:**

Design a circuit with three inputs (a, b, and c) and three outputs (f1, f2, and f3).

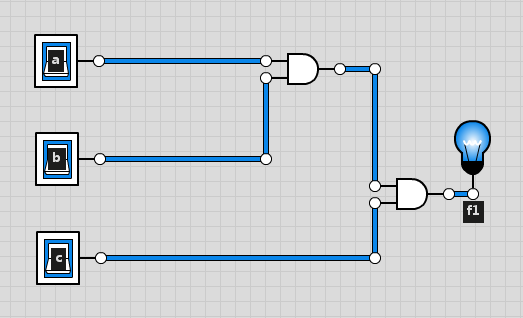
* The first output (f1) should only be true (1) when all three of the inputs are low.

**Logic function:**  **f = a’·b’·c’**

**Truth Table:**

|  |  |  |  |
| --- | --- | --- | --- |
| **a** | **b** | **c** | **f1** |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |

**Circuit graph** (with f1 only)**:**



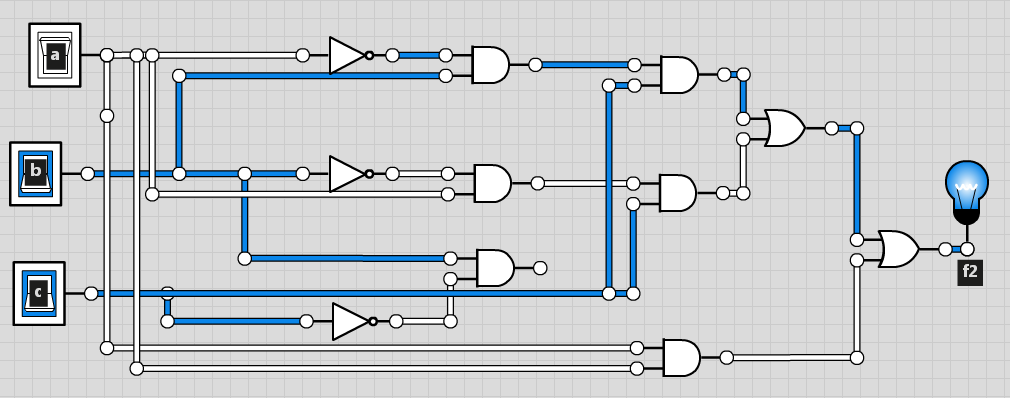
* The second output (f2) should only be true (1) when exactly two of the inputs are high.

**Logic function: f = a’·b·c + a·b’·c + a·b·c’**

**Truth Table:**

|  |  |  |  |
| --- | --- | --- | --- |
| **a** | **b** | **c** | **f2** |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

**Circuit graph** (with f2 only)**:**



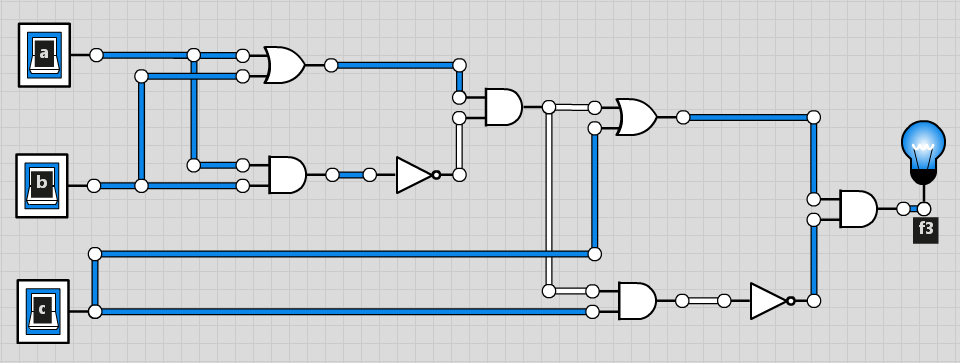
* The third output (f3) should be true (1) whenever an odd number of the inputs are high.

**Logic function:**  **f = a’·b·c’ + a’·b’·c + a·b’·c’ + a·b·c**

**Truth Table:**

|  |  |  |  |
| --- | --- | --- | --- |
| **a** | **b** | **c** | **f3** |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

**Circuit graph** (with f3 only)**:**



**Part III Circuit graph:**

